Amendments to the Claims

Please cancel Claims 1, 6, 9, 10 and 12-22. Please amend Claims 2, 4, 5, 7, 8 and 11. The Claim Listing below will replace all prior versions of the claims in the application:

Claim Listing

1. (Canceled)

2. (Currently Amended) [[The]] An apparatus ~~of claim 1, wherein~~ for processing or storing secure data comprising:

a secure port for transmitting and receiving secure data;

a test port for transmitting and receiving test data; and

a test mode entry circuit that causes entry of the apparatus into a test mode, the test mode entry circuit operable for a predetermined time period, the test mode entry circuit [[is]] being coupled to the secure port, ~~and when data is applied to the secure port,~~ the test mode entry circuit ~~causes~~ causing entry of the apparatus into a work mode when secure data is applied to the secure port.

3. (Original) The apparatus of claim 2, wherein the entry into the work mode disables re-entry of the apparatus to the test mode.

4. (Currently Amended) The apparatus of claim [[1]] 2, wherein the predetermined time period commences approximately coincident to when power is applied to the apparatus.

5. (Currently Amended) [[The]] An apparatus ~~of claim 1, further~~ for processing or storing secure data, comprising:

a secure port for transmitting and receiving secure data;

a test port for transmitting and receiving test data;

a test mode entry circuit that causes entry of the apparatus into a test mode, the test mode entry circuit operable for a predetermined time period; and

test circuitry coupled to the test mode entry ~~circuitry~~ circuit ~~which performs~~ , the test circuitry performing diagnostic functions while the apparatus is in the test mode.

6. (Canceled)

7. (Currently Amended) [[The]] An apparatus ~~of claim 6, wherein~~ for processing or storing secure data, comprising:

a secure port for transmitting and receiving secure data;

a test port for transmitting and receiving test data; and

a test mode entry circuit that causes entry of the apparatus into a test mode, the test mode entry circuit operable for a predetermined time period, the test mode entry circuit being coupled to the test port, entry into the test mode being dependent on test data received through the test port within the predetermined time period, the test data ~~comprises~~ comprising one or more electrical signals received through the test port and at least one of the electrical signals [[is]] being an out of [[spec]] static super voltage.

8. (Currently Amended) [[The]] An apparatus ~~of claim 6, wherein~~ for processing or storing secure data, comprising:

a secure port for transmitting and receiving secure data;

a test port for transmitting and receiving test data; and

a test mode entry circuit that causes entry of the apparatus into a test mode, the test mode entry circuit operable for a predetermined time period, the test mode entry circuit ~~causes~~ causing the apparatus to enter [[the]] a work mode if [[the]] no test data is [[not]] received within the predetermined time period.

9, 10 (Canceled)

11. (Currently Amended) [[The]] An apparatus ~~of claim 10, further~~ for processing or storing secure data, comprising:

a secure port for transmitting and receiving secure data;

a test port for transmitting and receiving test data;

a test mode entry circuit that causes entry of the apparatus into a test mode, the test mode entry circuit operable for a predetermined time period,

non-volatile memory for storing the secure data; and

a memory erasing circuit ~~which erases~~ for erasing the secure data stored in the non-volatile memory upon entry of the apparatus into the test mode.

12-22 (Canceled)